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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,154	04/01/2004	Blaine Douglas Gaither	10001399-2	7372

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Intellectual Property Administration
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EXAMINER

ELLIS, KEVIN L

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/814,154

Applicant(s)

GAITHER, BLAINE DOUGLAS

Examiner

Kevin L. Ellis

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 March 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-4 and 9-18 is/are allowed.
- 6) ☒ Claim(s) 5-7, 19 and 21 is/are rejected.
- 7) ☒ Claim(s) 8, 20 and 22 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____

Art Unit: 2188

Detailed Action

1. Claims 1-22 are presented for examination. The current application is a continuation of application serial number 09/733,123, now U.S. Patent No. 6,721,848.

Claim Rejections – 35 USC § 112

2. Claim 21 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- A) Claim 21 recites: "the intermediary cache" and "the associated local caches" (Lines 1-2) has unclear antecedent basis.

Claim Rejections – 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 5-7 and 19 are rejected under 35 U.S.C. § 102(e) as being anticipated by Cherabuddi et al., U.S. Patent 5,996,048.

- A) As to claim 5, Cherabuddi et al. discloses the invention as claimed. There is a method for reducing processing time and bus bandwidth during snoop processing of a multi-processor computer architecture (see Abstract and Col 3 Lines 23-30), the architecture comprising higher level caches (Fig 1 Ref 30 & 32 and Col 2 Line 2) and intermediary caches (Fig 1 Ref 34 and Col 2 Line 3), comprising establishing the intermediary caches as inclusive caches (Col 2 Line 57, Col 3 Lines 40-65, and Col 4 Lines 22-36), wherein an inclusive intermediary cache includes at least all memory lines of corresponding higher level caches (see Col 3 Lines 40-65 and Col 4 Lines 22-36), presenting a virtual address for a memory line on a virtually-addressed bus (this bus would be internal to the processor to send data and addresses to the virtual first level cache), initiating snoop processing of the intermediary caches (upon a first microprocessor not finding the data in its L1 or L2 cache a snoop would be performed upon the other caches, see Figs 4A-4C and Col 3 Lines 9-18), if receiving a snoop hit, initiating snoop processing on the higher level caches (see Col 4 Lines 22-40), if receiving a snoop miss, accessing main memory (this is the normal behavior when a snoop miss occurs, the data is present in the main memory, see Col 4 Lines 25-26).
- B) As to claim 6, the intermediary caches do exceed the total capacity of any higher level caches (see Col 2 Line 57).
- C) As to claim 7, any line of data evicted from the intermediary cache is also evicted from the upper level caches (see Col 4 Line 56 to Col 5 Line 15).
- D) As to claim 19, Cherabuddi et al. discloses the invention as claimed. There is a mechanism for translating from a virtual bus to a physical interconnect (see Col 2 Lines

Art Unit: 2188

2-3 and Col 5 Lines 42-50), a main memory storing memory lines (Fig 1 Ref 26), processors coupled to the main memory and capable of accessing the memory lines (see Fig 1 Ref 12, 14, and 16), and means for reducing processing time and bus bandwidth during snoop processing by the processors (see Abstract, Col 2 Lines 48-58, Col 2 Line 57, Col 3 Lines 23-30).

Allowable Claims

5. Claims 1-4 and 9-18 are allowed.
6. Claims 8 and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

7. Applicant's arguments with respect to claims 5-7 and 19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin L. Ellis whose telephone number is 571-272-4205. The examiner can normally be reached on weekdays from weekdays from 6:00AM-2:30PM.

Art Unit: 2188

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kevin L. Ellis
Primary Examiner
May 31, 2005

